# CLOCK SKEW PREVENTING CIRCUIT

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## Abstract

PROBLEM TO BE SOLVED: To output a clock signal having no clock skew by inputting clock signals having clock skews and to prevent the waveform of the outputted clock signal from being weakened. SOLUTION: This circuit is equipped with plural input lines 11a, 11b, and 11c for inputting plural clock signals and also equipped with a logic circuit 14 which inputs the plural clock signals and outputs a clock signal synchronized with the slowest clock signal among them. Then this circuit is equipped with output lines 17a, 17b, and 17c which input the clock signal outputted from this logic circuit 14 to a buffer and output plural clock signals.